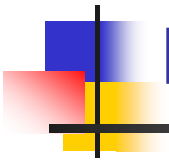
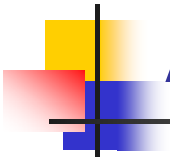


Introduction to Sequential Devices



Agenda

- Models for Sequential Circuit
- Memory Devices
- Latches
- Flip-flops

Models for Sequential Devices

- Block Diagram Representation

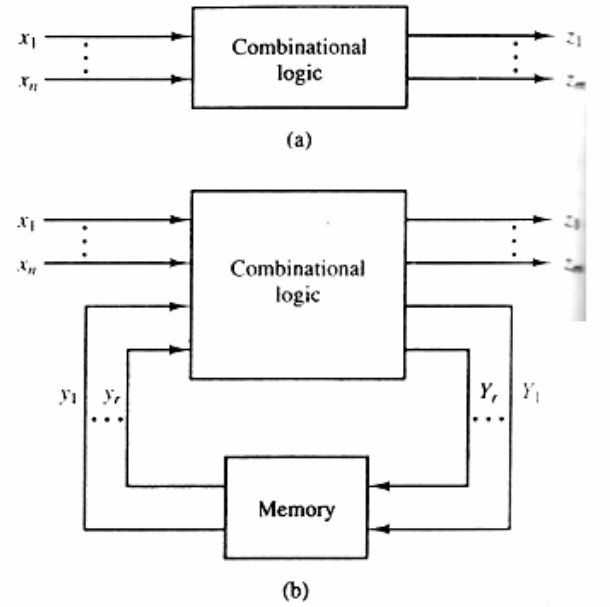
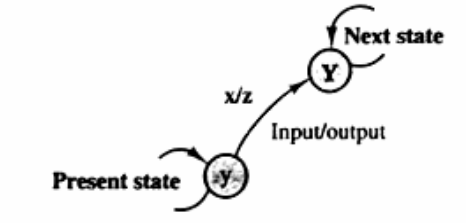
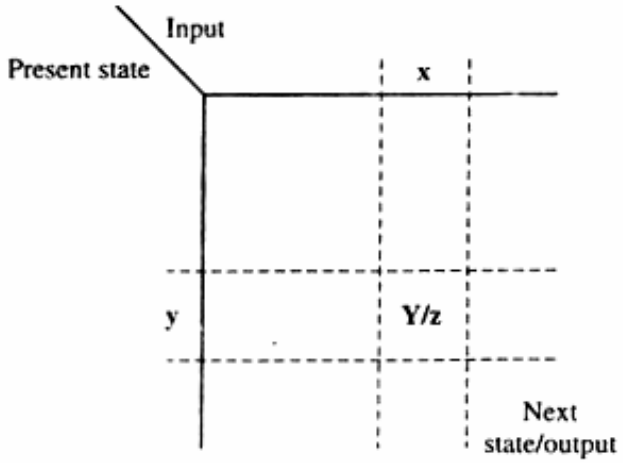


Figure 6.1 The sequential circuit model. **(a)** Combinational logic circuit. **(b)** Sequential logic circuit.

Models for Sequential Devices

- State Tables and Diagram





Models for Sequential Devices

- 1 input variable *x*, 2 state variable *y1* and *y2*, and 1 output variable *z*.

Inputs:	$x = 0$
	$x = 1$
States:	$[y_1, y_2] = [00] \equiv A$
	$[y_1, y_2] = [01] \equiv B$
	$[y_1, y_2] = [10] \equiv C$
	$[y_1, y_2] = [11] \equiv D$
Outputs:	$z = 0$
	$z = 1$

Models for Sequential Devices

Present state	Input x = 0	Input x = 1
A	$D/0$	$C/1$
B	$B/1$	$A/0$
C	$C/1$	$D/0$
D	$A/0$	$B/1$

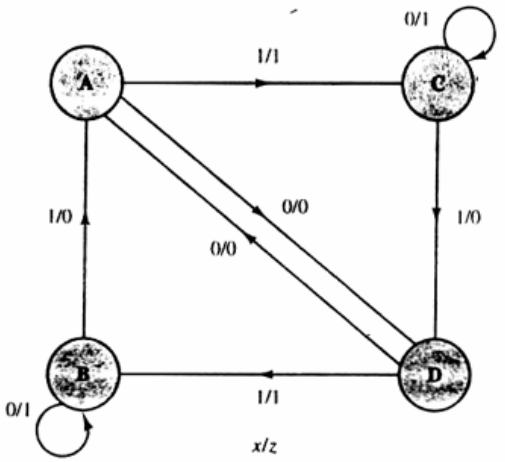
$x = 0110101100$

The circuit will behave as follows when the initial state is A:

Time:	0	1	2	3	4	5	6	7
Present state:	A	D	B	A	D	B	B	A
Input:	0	1	1	0	1	0	1	1
Next state:	D	B	A	D	B	B	A	C
Output:	0	1	0	0	1	1	0	1

Hence, this input sequence applied to the machine in state A sequence

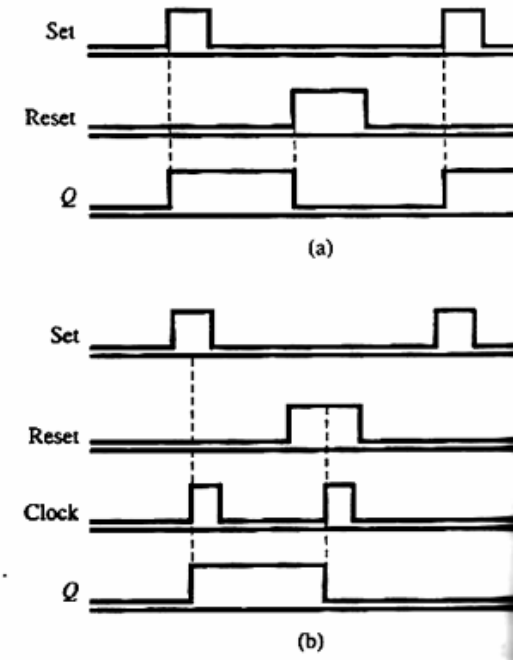
$z = 0100110111$



Memory Devices

- The two element types most commonly used in switching circuits are *latch* and *flip-flop*.
- Latch is a memory element whose excitation input signals control the state of the devices.
- Flip-flop differs from a latch in that it has control signal called a *clock*.

Memory Devices



a) Latch responds immediately to excitation.

b) Flip-flop responds only on a clock signal.

Latch

- Set-Reset Latch

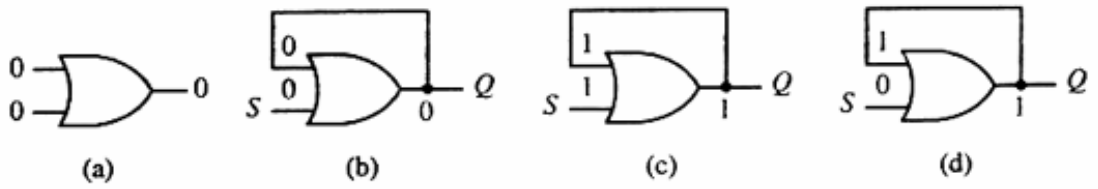
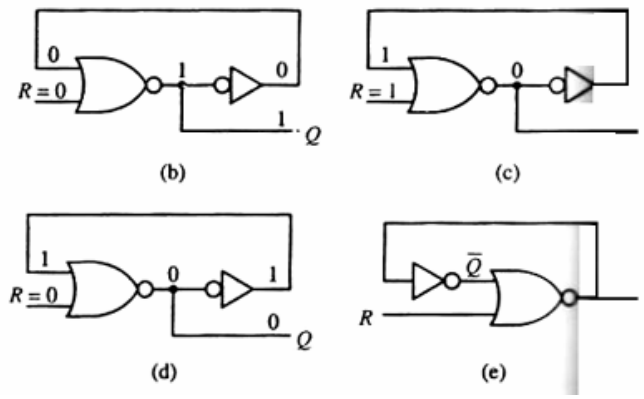
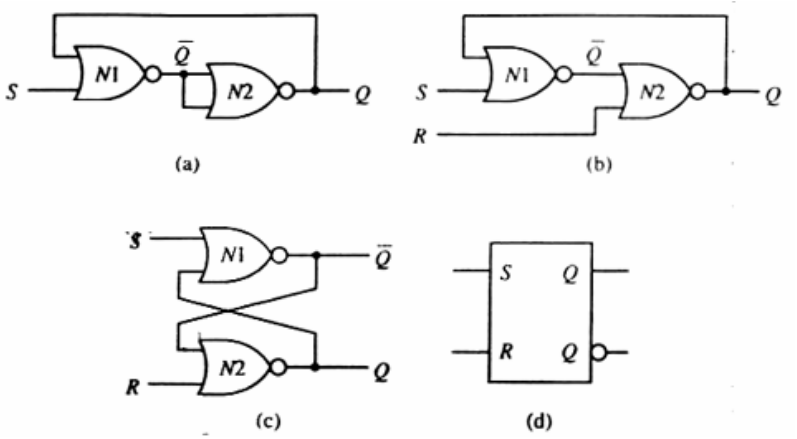


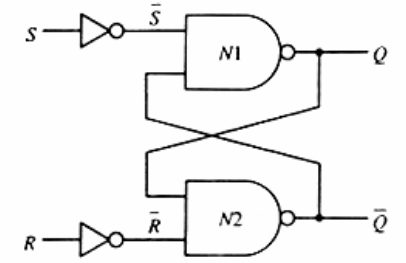
Figure 6.5 Set latch. **(a)** OR gate. **(b)** Feedback added. **(c)** Output set to 1. **(d)** Feedback holds Q = 1.

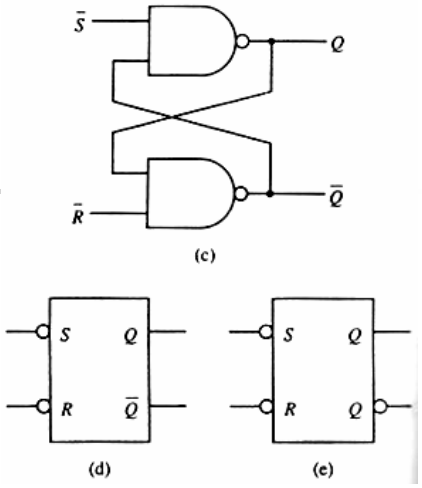
Latch

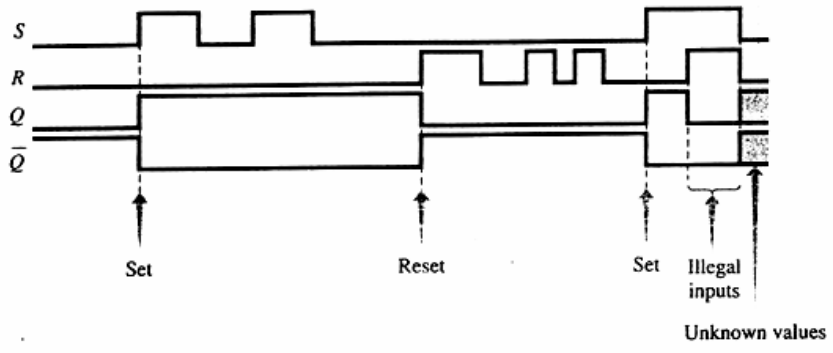




Latch





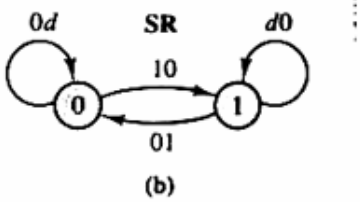


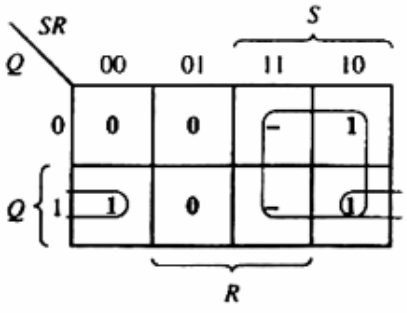
Latch

- SR Latch Excitation table

Excitation inputs S	R	Present state Q	Next state Q*	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	×	Not allowed
1	1	1	×	

(a)

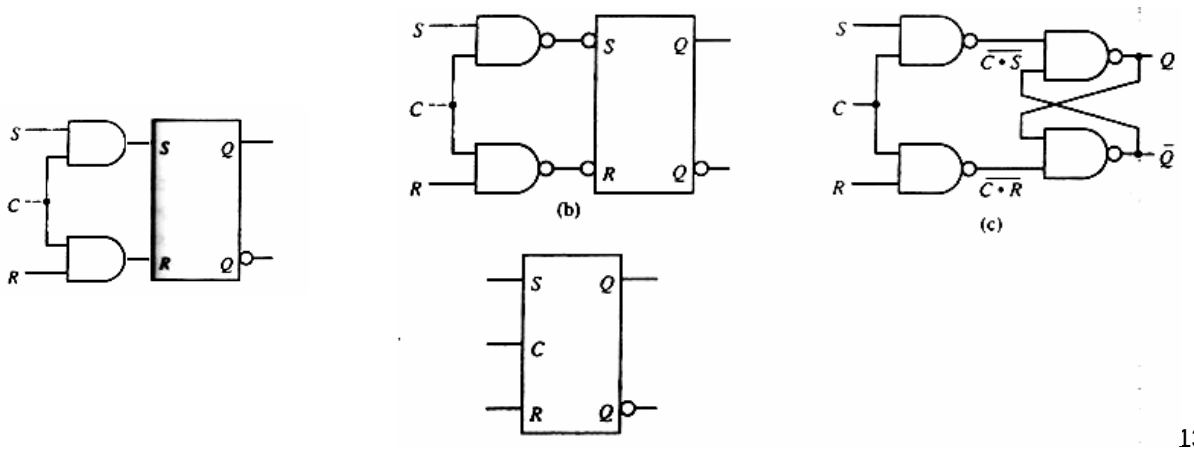




$$Q^* = S + \bar{R}Q$$

Latch

- Gate SR Latch
  - A control signal, *C*, is added to an SR latch to apply the inputs *S* and *R*.

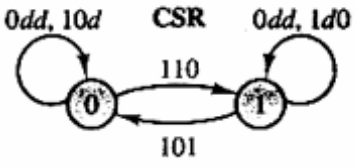


Latch

Enable inputs	Excitation inputs		Present state	Next state	
C	*S*	*R*	*Q*	*Q**	
0	×	×	0	0	Hold
0	×	×	1	1	
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	×	Not allowed
1	1	1	1	×	

(a)

$$Q^* = SC + \bar{R}Q + \bar{C}Q$$



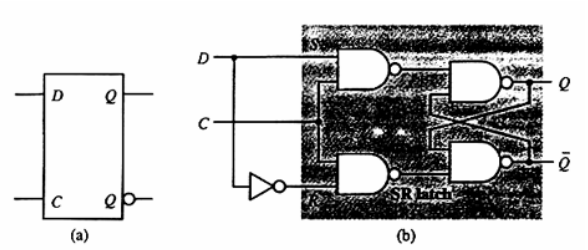
(b)

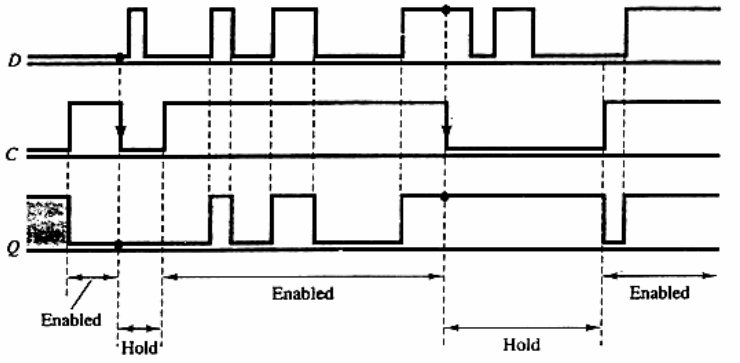
Figure 6.14 Gated SR latch characteristics. **(a)** Excitation table. **(b)** State diagram.

Latch

- Delay Latch

Enable input C	Excitation input D	Present state Q	Next state Q*	
0	×	0	0	Hold
0	×	1	1	
1	0	0	0	Store 0
1	0	1	0	
1	1	0	1	Store 1
1	1	1	1	

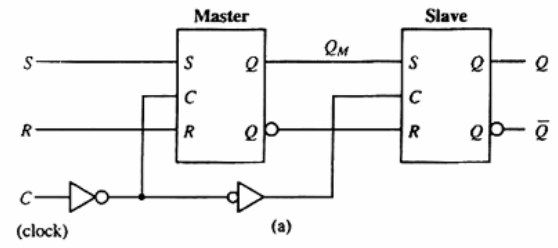


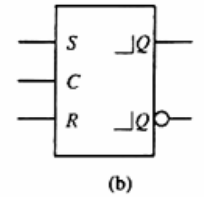


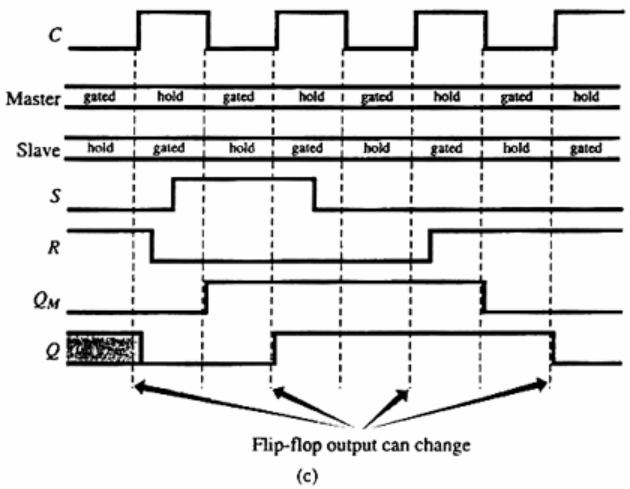
$$Q^* = SC + \bar{R}Q + \bar{C}Q$$
$$= DC + (\bar{\bar{D}})Q + \bar{C}Q$$
$$= DC + DQ + \bar{C}Q$$
$$= DC + \bar{C}Q$$

Flip-flop

- Master-Slave SR Flip-flop







Flip-flop

- Master-Slave SR Flip-flop

S	R	Q	C	Q^*	
0	0	0	⎍	0	No change
0	0	1	⎍	1	
0	1	0	⎍	0	Reset
0	1	1	⎍	0	
1	0	0	⎍	1	Set
1	0	1	⎍	1	
1	1	0	⎍	×	Not allowed
1	1	1	⎍	×	

(a)

$$Q^* = S + \bar{R}Q$$

Flip-flop

- Master-Slave D Flip-flop

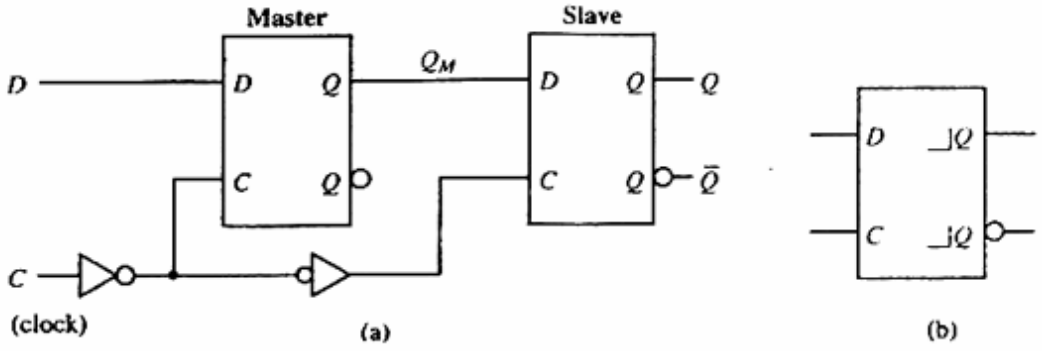


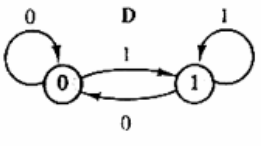
Figure 6.23 Master-slave D flip-flop. **(a)** Logic diagram. **(b)** Logic symbol.

Flip-flop

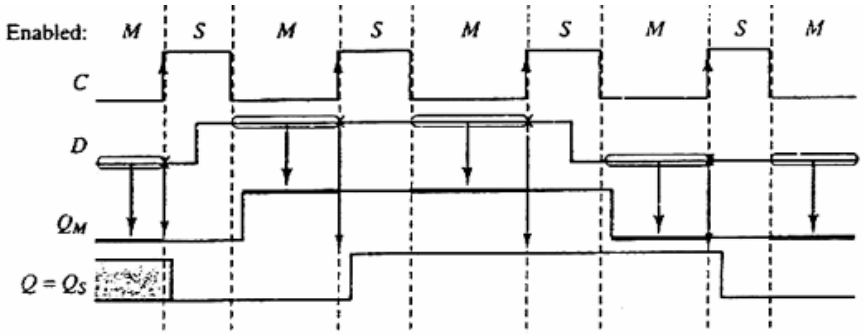
$$Q^* = D$$

D	Q	C	Q*	
0	0	⎍	0	Store 0
0	1	⎍	0	
1	0	⎍	1	Store 1
1	1	⎍	1	

(a)



(b)



(c)

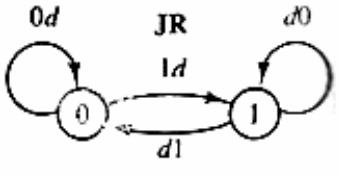
Figure 6.24 Master-slave D flip-flop characteristics. **(a)** Excitation table. **(b)** State diagram. **(c)** Timing diagram.

Flip-flop

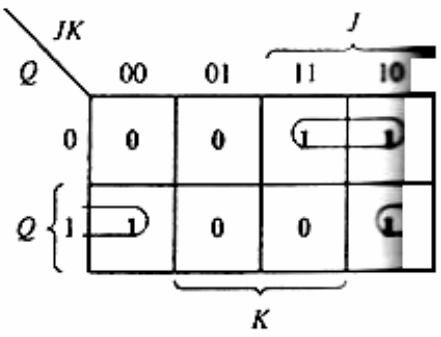
- Master-Slave JK Flip-flop

J	K	Q	C	Q*	
0	0	0	⎍	0	Hold
0	0	1	⎍	1	
0	1	0	⎍	0	Reset
0	1	1	⎍	0	
1	0	0	⎍	1	Set
1	0	1	⎍	1	
1	1	0	⎍	1	Toggle
1	1	1	⎍	0	

(a)



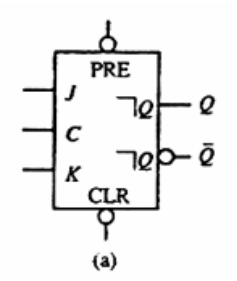
(b)

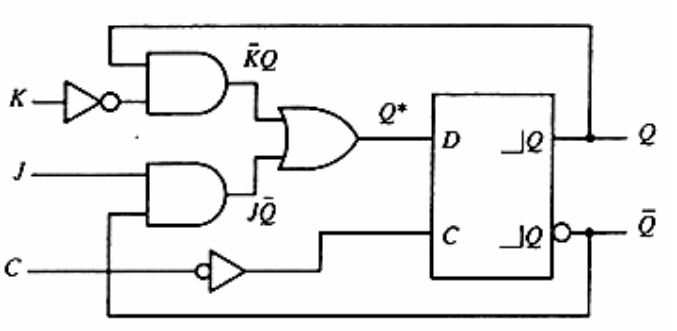


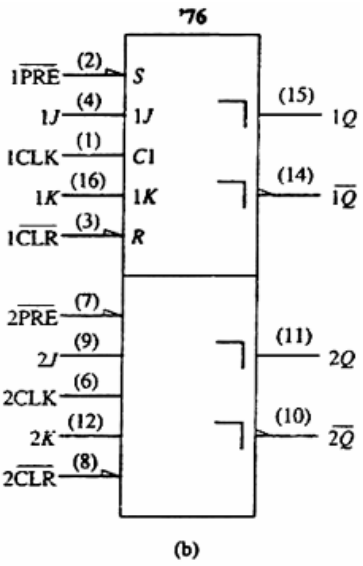
$$Q^* = \bar{K}Q + J\bar{Q}$$

Flip-flop

- Master-Slave JK Flip-flop







Flip-flop

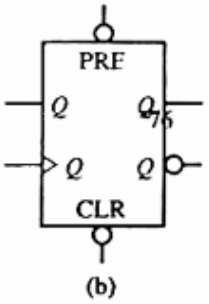
- Edge-triggered D Flip-flop
  - Called *positive edge triggered*, if it responds to a 0→1 clock transition.
  - Called *Negative edge triggered*, if it responds to a 1→0 clock transition
  - Special pin, *PRE* and *CLR*, for Asynchronous Set and Reset (without Clock).

Flip-flop

- 7474 Dual Positive-edge-triggered D Flip-flop Module

Inputs				Outputs		
$\overline{PRE}$	$\overline{CLR}$	D	CLK	Q	$\overline{Q}$	Mode
L	H	×	×	H	L	Set
H	L	×	×	L	H	Clear
L	L	×	×	H	H	Not allow
H	H	H	↑	H	L	Clocked ope
H	H	L	↑	L	H	Clocked ope
H	H	×	L	Q_0	$\overline{Q}_0$	Hold

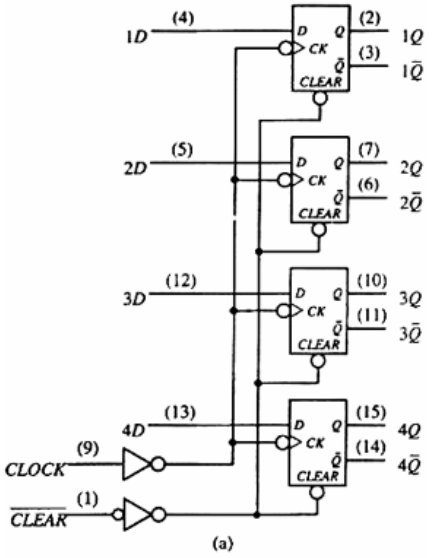
Figure 6.29 SN7474 excitation table
Book Volume 2, Texas Instruments Inc.,



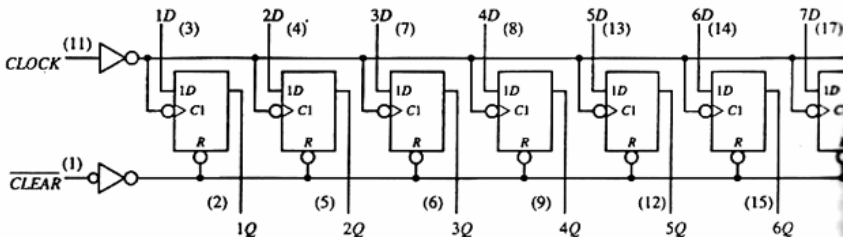
(b)

Flip-flop

- 74175 and 74273 Dual Positive-edge-triggered D Flip-flop Module

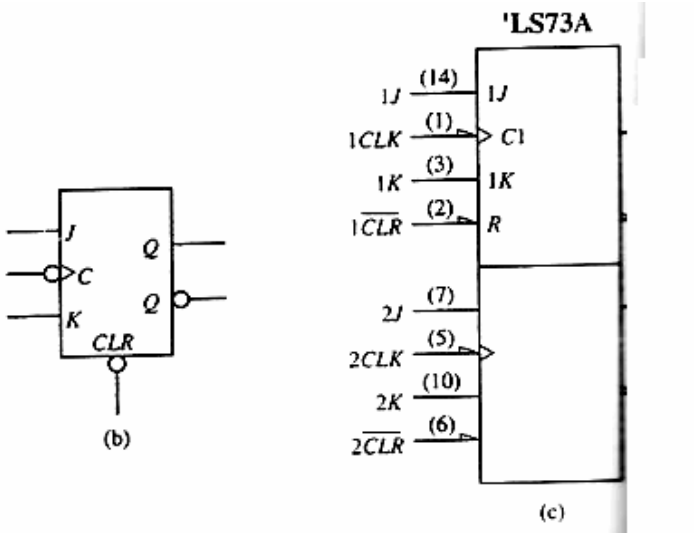


(a)



Flip-flop

- 7473 Dual Positive-edge-triggered JK Flip-flop Module

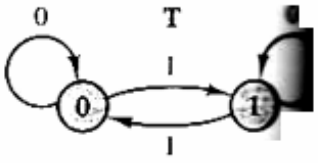


Flip-flop

- Edge-triggered T (trigger or toggle) Flip-flop
  - Used in sequential logic circuit that counts pulse on a signal line.

T	Q	Q*	
↑	0	1	Toggle
↑	1	0	Toggle

(a)



$Q^* = \bar{Q}$

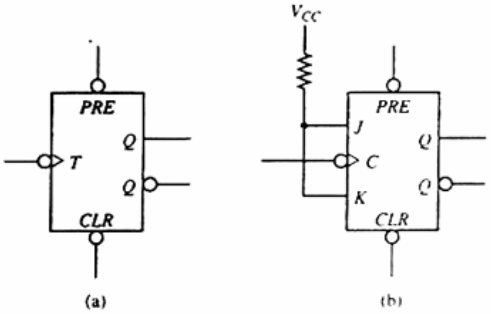
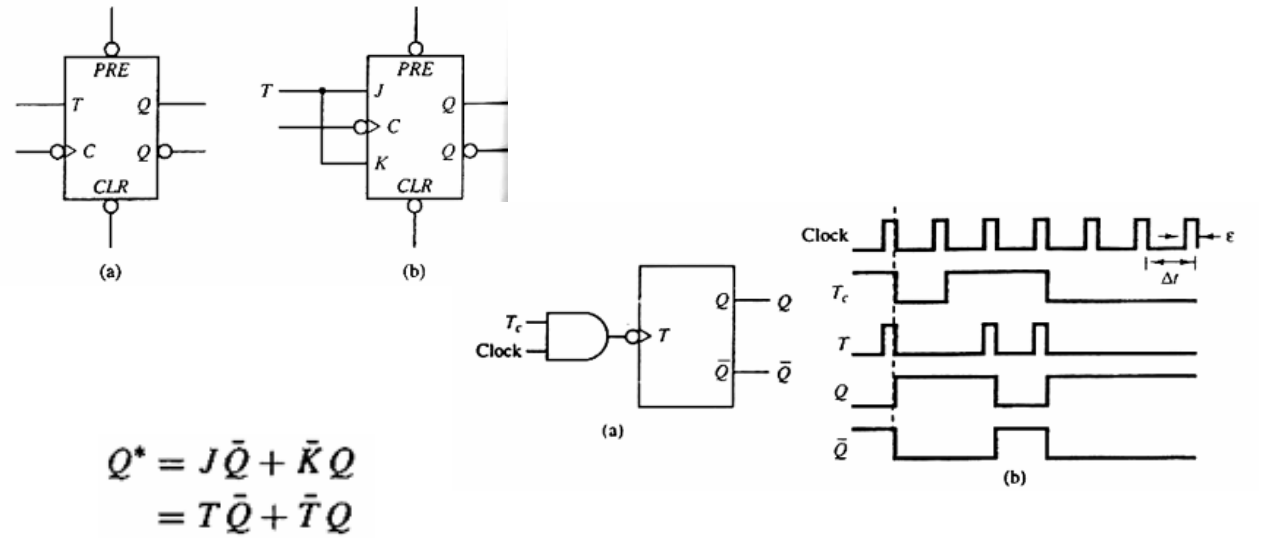


Figure 6.34 Edge-triggered T flip-flop characteris
(a) Excitation table. **(b)** State diagram.

Flip-flop

- Clocked T Flip-flop



$$Q^* = J\bar{Q} + \bar{K}Q$$
$$= T\bar{Q} + \bar{T}Q$$

Flip-flop

- Latch and Flip-flop Summary

TABLE 6.3 SUMMARY OF LATCH AND FLIP-FLOP CHARACTERISTICS

Device	Characteristic Equation
SR latch	$Q^* = S + \bar{R}Q$
Gated SR latch	$Q^* = SC + \bar{Q}R + \bar{C}Q$
D latch	$Q^* = DC + \bar{C}Q$
SR flip-flop	$Q^* = S + \bar{R}Q$
D flip-flop	$Q^* = D$
JK flip-flop	$Q^* = \bar{K}Q + J\bar{Q}$
T flip-flop (edge-triggered)	$Q^* = \bar{Q}$
T flip-flop (clocked)	$Q^* = T\bar{Q} + \bar{T}Q$